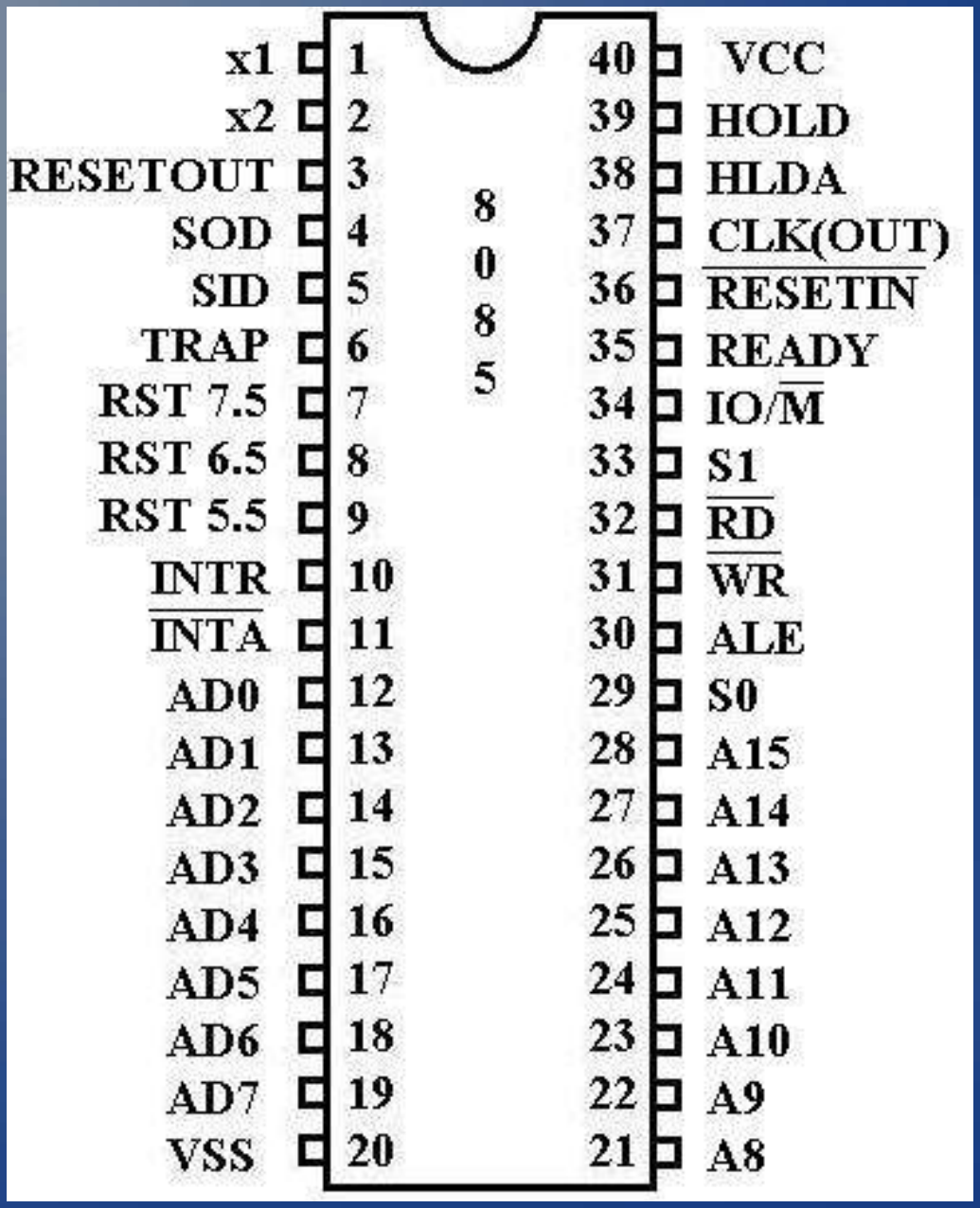
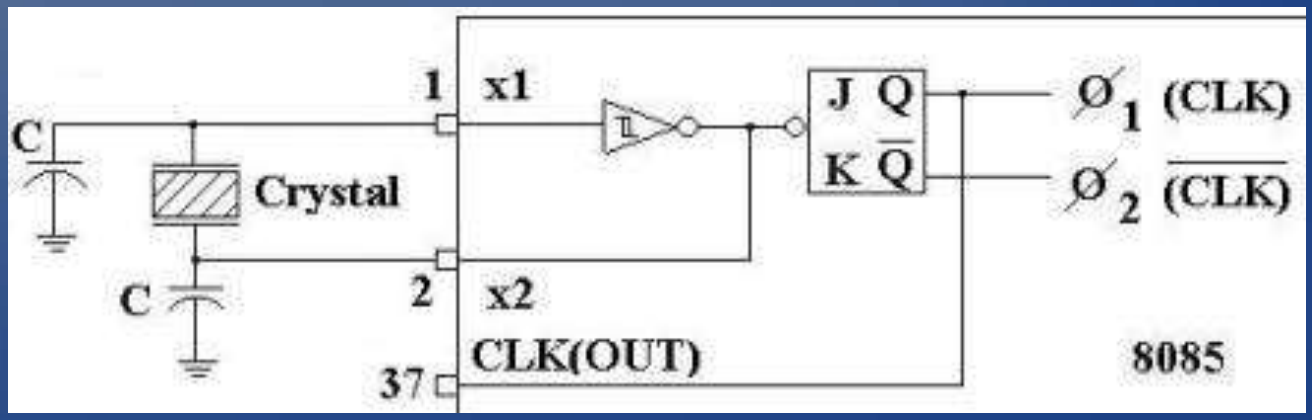
Chapter 3
The Intel 8085 Microprocessor


8085
x1 1
x2 2
RESETOUT 3
SOD 4
SID 5
TRAP 6
RST 7.5 7
RST 6.5 8
RST 5.5 9
INTR 10
INTA 11
AD0 12
AD1 13
AD2 14
AD3 15
AD4 16
AD5 17
AD6 18
AD7 19
VSS 20
40 VCC
39 HOLD
38 HLDA
37 CLK(OUT)
36 RESETIN
35 READY
34 IO/M
33 S1
32 RD
31 WR
30 ALE
29 S0
28 A15
27 A14
26 A13
25 A12
24 A11
23 A10
22 A9
21 A8

Pins : 1, 2 and 37

The data sheet of an 8085 specifies the limits on the clock frequency f_{min} = 500 kHz , f_{max} = 3.125 MHz. When a crystal is connected to the x1 and x2 inputs, it determines the frequency of the on-chip oscillator. The oscillator output Schmitt trigger drives a flip-flop that provides two clock signals 10 and 20 These signals drive the internal 8085 circuits. The CLK signal also goes to pin 37 to drive peripheral chips. Because the flip-flop divides by 2, the clock frequency is half the driving frequency of the timing element.



C : 10-20 pF , Crystal : 1-6.25 MHz

Pin : 3

This pin carries the RESET OUT signal. When high, it indicates that the CPU is being reset; that is, the program counter, instruction register and so on are being reset to zero. The RESET OUT signal goes to peripheral chips. When you first power up. The whole system including the 8085 and peripheral chips is reset or initialised. After the RESET OUT goes low, the processing begins.

Pins : 4 and 5

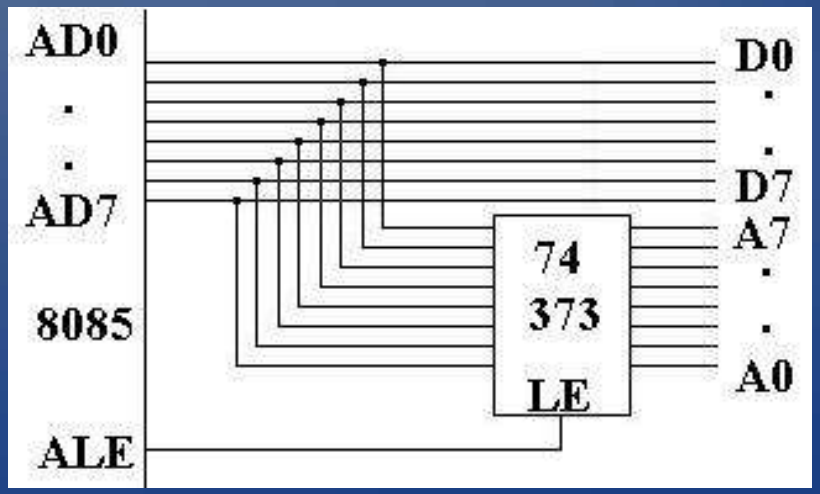
SOD stands for serial out data. SID stands for serial in data.

Pins : 6 to 11

These pins are part of the interrupt control unit. The 8085 has five inputs for interrupt requests. Pins 6 to 10 are input pins for interrupt signals. Pin 11 is an output with a signal called the interrupt acknowledge (INTA).

Pins : 12 to 19 and 30

Pins 12 to 19 carry the lower 8 address bits or the 8 data bits. The work properly it needs one more memory chips connected to it. Each memory chip has its own MAR (memory-address register) usually called an address latch. This latch stores the incoming address from the address bus and address-data bus. ALE stands for address latch enable. The falling edge of the ALE signal strobes (loads) the address on the address bus.



Pin : 20

Vss is the system ground.

Pins : 21 to 28

These pins are the rest of the address bus.

Pins : 29 and 33

Pins 29 and 33 carry output signals known as status signals. Labeled S_0 and S_1.

s0	s1	state
0	0	HALT
0	1	READ
1	0	WRITE
1	1	FETCH

Pins : 31, 32 and 34

These three pins function together. They are connected to memory and I/O chips. A low I0/M indicates a memory operation and a high 10/M means that an I/O instruction is being executed.

The RD and WR determine whether a read or a write is done. A low WR means a write operation and a low RD means a read operation. They are never both low at the same time.

Pin : 35

Some peripheral devices are slow; they are unable to run at the same speed at the 8085. One way to slow down the 8085 is with the READY signal. The 8085 address a peripheral device. If the device is not ready it will return a low READY bit to the 8085. Then the 8085 generates a number of T states called WAIT states. When the peripheral device is ready it will send a high READY signal to the 8085. Then the 8085 can complete the data transfer. The action is a form of handshaking.

Pin : 36

Pin 36 is an input carrying the RESET IN signal. When it is slow the CPU will reset the program counter, instruction register and other circuits. It also sends a high RESET OUT to pin 3. The CPU remains in reset until the RESET IN signal goes high. Then the data processing begins.

Pins : 38 and 39

The HOLD and HLDA (hold acknowledge) are used in DMA (direct memory access) operations.

Pin : 40

It connects to a source of +5V. The tolerance on the supply voltage is ±5 percent. The power dissipation is less than 1.5 W.

3 – 2 Interrupts

RST 0 to RST 7 are software restarts because they are instructions. Besides these software restarts, the 8085 has four hardware restarts designated TRAP (pin 6), RST 7.5 (pin 7), RST 6.5 (pin 8), and RST 5.5 (pin 9). When any of these pins is active, the internal circuits of the 8085 produce a hardware CALL to a predetermined vector location.

A hardware call like this is known as a *vectored interrupt* because the program branches to a vector location where the starting address of a service subroutine is stored. By connecting the hardware restart pins to peripheral devices, we can use interrupt-driven I/O instead of programmed I/O. Table 3-2 shows the interrupts and vectored locations.

Restart	Vector Location
RST 0	0000H
RST 1	0008H
RST 2	0010H
RST 3	0018H
RST 4	0020H
TRAP	0024H
RST 5	0028H
RST5.5	002CH
RST 6	0030H
RST6.5	0034H
RST 7	0038H
RST7.5	003CH

Interrupt	Priority	Vector Location
TRAP	1	0024H
RST 7.5	2	003CH
RST 6.5	3	0034H
RST 5.5	4	002CH
INTR	5	None

Figure 3-4 Interrupt respond

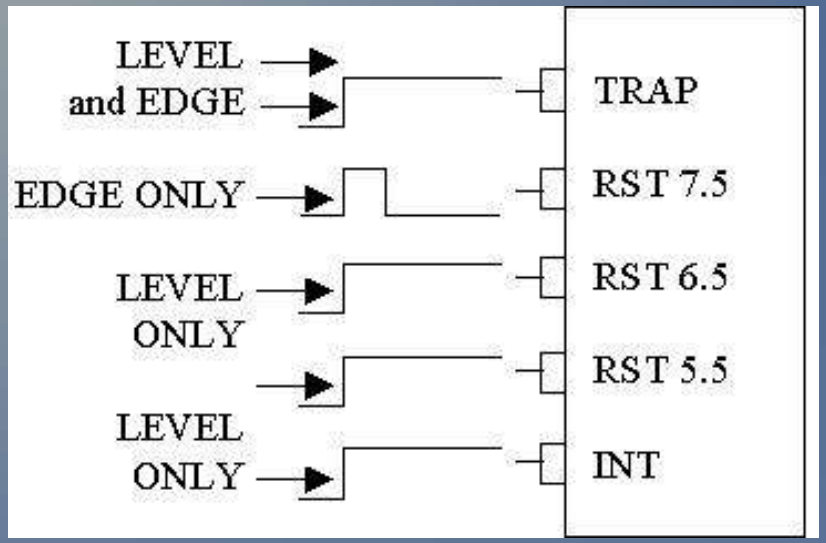
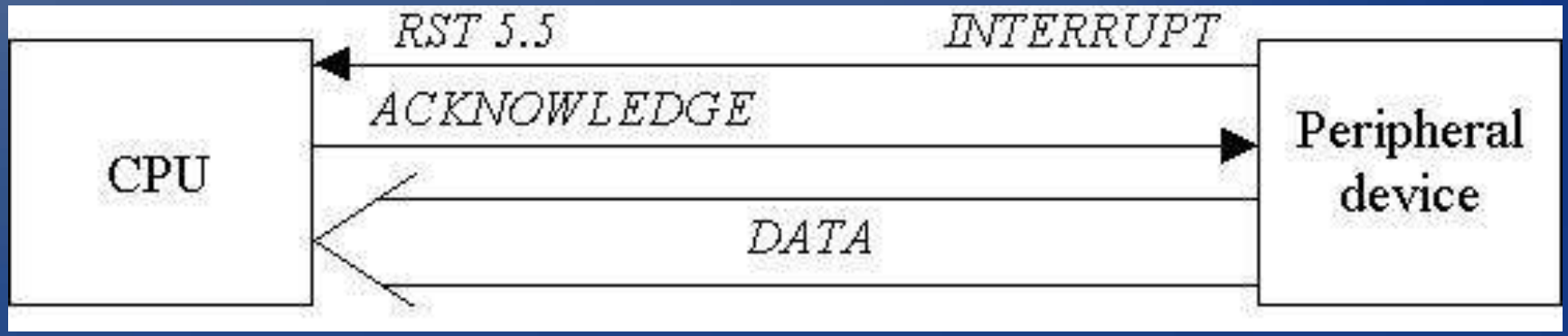
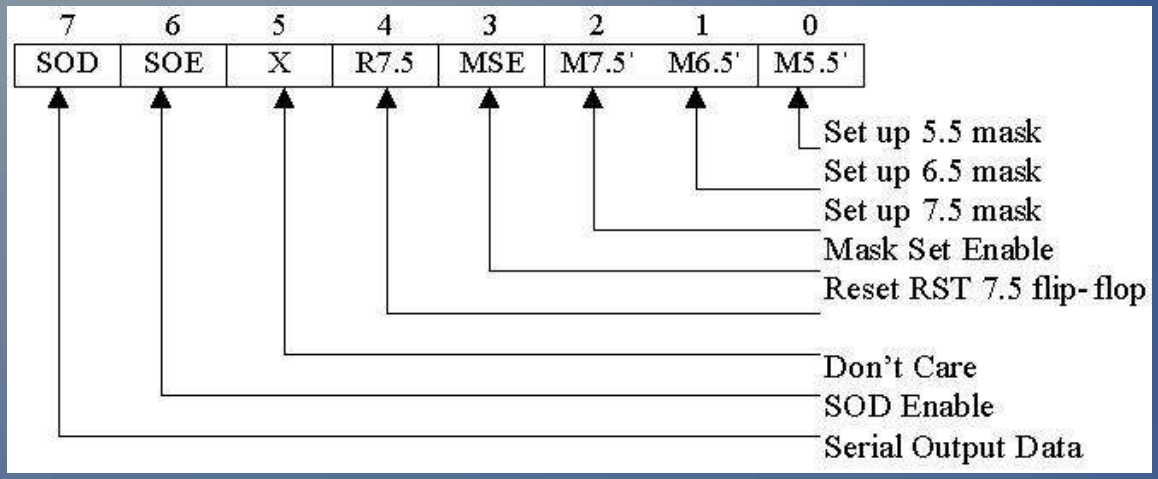


Figure 3-5 Interrupt Driven I/O



3.4. Interrupt Instructions *EI , DI, SIM and RIM*

SIM stands for set interrupt mask



RIM stands for read interrupt mask.