Chapter 2

The Intel 8080

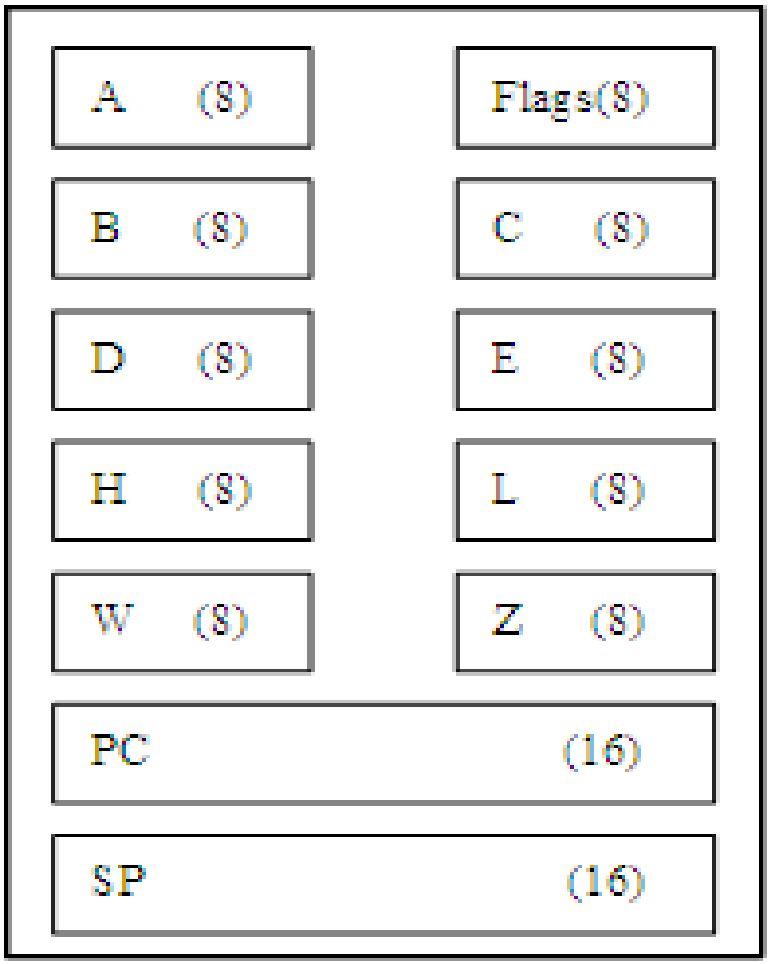

Figure 2.1 The registers of the Intel 8080 microprocessor

Flags:

Zero Flag : If the result of an operation has the value 0, the flag is set to a 1 otherwise it is reset to a 0.

Sign Flag : If the most significant bit of the result of the operation is a 1, the flag is set to a 1 otherwise it is reset to a 0.

Parity Flag : If the bits of the result of an operation have even parity the flag is set to a 1,otherwise it is reset to a 0.

Carry Flag : If the last arithmetic operation resulted in a carry or a borrow out of the high-order bit the flag is set to a 1, otherwise it is reset to a 0.

Auxiliary Carry Flag : If an addition causes a carry out of bit 3 and into bit 4 of the resulting value the flag is set to 1 otherwise it is reset to a 0

Table 2.1 The Intel 8080 instruction format

	Byte 1	Byte 2	Byte 3
Single Byte	op code	-	-
Two Byte	op code	Data or Address	-
Three Byte	op code	Low Byte of Data or Address	High Byte of Data or Address

Table 2.2 (a) Bit patterns of registers (b) Bit patterns of register pairs

Register	Code
A	111
B	000
C	001
D	010
E	011
H	100
L	101

(a)

Register Pair	Code
B (BC)	00
D (DE)	01
H (HL)	10
SP	11

(b)

8080 Micropocessor Instruction Set

1. Data Transfer Group
2. Arithmetic Group
3. Logic Group
4. Branch Group
5. Stack, I/O and Machine Control Group

Instruction Set

1. Data Transfer Group

MOV r1,r2 (MOVe from register 2 to register 1)
MVI r, nn (MoVe Immediate to register)
LXI rp, nnnn (Load Immediate to register pair, X shows a 16 bit operation)
LDA nnnn (LoaD Accumulator direct)
STA nnnn (STore Accumulator direct)
LHLD nnnn (Load H and L Direct)
SHLD nnnn (Store H and L Direct)
LDAX rp (LoaD Accumulator indirect)
STAX RP (STore Accumulator indirect)
XCHG (eXCHanGe H and L with D and E)

Instruction Set

2. Arithmetic Group

ADD r (ADD accumulator with register)
ADI nn (ADd Immediate)
ADC r (ADd register with Carry)
ACI nn (Add with Carry Immediate)
SUB r (SUBtract register)
SUI nn (SUbtract Immediate)
SBB r (Subtract register with borrow)
SBI nn (Subtract with Borrow Immediate)
DAD rp (Double register Add)
RAL (Rotate Accumulator Left)
RAR (Rotate Accumulator Right)
RLC (Rotate Left through Carry)
RRC (Rotate Right through Carry)

Instruction Set

2. Arithmetic Group

INR r	(INcRement register)
INX rp	(INcrement register pair)
DCR r	(DeCRement register)
DCR M	(DeCRement memory)
DCX rp	(DeCrement register pair)
CMA	(CoMplement A)
STC	(SeT Carry flag)
CMC	(CoMplement Carry flag)
DAA	(Decimal Adjust Accumulator)

Instruction Set

3. Logic Group

ANA r	(ANd A with register)
ANI nn	(ANd Immediate)
XRA r	(eXclusive oR A with register)
XRI nn	(eXclusive oR A Immediate)
ORA r	(OR A with register)
ORI nn	(OR Immediate)
CMP r	(CoMPare register)
CPI nn	(CoMPare Immediate)

Instruction Set

4. Branch Group

JMP nnnn (JuMP)
J(FLAG) nnnn (Jump conditional)

Instruction	Op-code	Condition	Hex
JNZ	11000010	JUMP NOT ZERO (Z=0)	C2
JZ	11001010	JUMP ZERO (Z=1)	CA
JNC	11010010	JUMP NO CARRY (CY=0)	D2
JC	11011010	JUMP CARRY (CY=1)	DA
JPO	11100010	JUMP PARITY ODD (P=0)	E2
JPE	11101010	JUMP PARITY EVEN (P=1)	EA
JP	11110010	JUMP POSITIVE (S=0)	F2
JM	11111010	JUMP MINUS (S=1)	FA

Instruction Set

4. Branch Group

PCHL		(move H and L to PC)
CALL	nnnn	(CALL subroutine immediate)
C (FLAG)	nnnn	(Call subroutine conditional)

Instruction	Op-code	Condition	Hex
CNZ	11000100	CALL NOT ZERO (Z=0)	C4
CZ	11001100	CALL ZERO (Z=1)	CC
CNC	11010100	CALL NO CARRY (CY=0)	D4
CC	11011100	CALL CARRY (CY=1)	DC
CPO	11100100	CALL PARITY ODD (P=0)	E4
CPE	11101100	CALL PARITY EVEN (P=1)	EC
CP	11110100	CALL POSITIVE (S=0)	F4
CM	11111100	CALL MINUS (S=1)	FC

Instruction Set

4. Branch Group

RET (RETurn immediate)
R (FLAG) (Return conditional)

Instruction	Op-code	Condition	Hex
RNZ	11000000	CALL NOT ZERO (Z=0)	C0
RZ	11001000	CALL ZERO (Z=1)	C8
RNC	11010000	CALL NO CARRY (CY=0)	D0
RC	11001000	CALL CARRY (CY=1)	D8
RPO	11100000	CALL PARITY ODD (P=0)	E0
RPE	11101000	CALL PARITY EVEN(P=1)	E8
RP	11110000	CALL POSITIVE (S=0)	F0
RM	11111000	CALL MINUS (S=1)	F8

Instruction Set

4. Branch Group

RST (ReSTart)

Instructions	Op-code	Hex	jump address
RST 0	11000111	C7	0000 H
RST 1	11001111	CF	0008 H
RST 2	11010111	D7	0010 H
RST 3	11011111	DF	0018 H
RST 4	11100111	E7	0020 H
RST 5	11101111	EF	0028 H
RST 6	11110111	F7	0030 H
RST 7	11111111	FF	0038 H

Instruction Set

5. Stack, I/O and Machine Control Group

PUSH	rp	(PUSH register pair)
POP	rp	(POP register pair)
XTHL		(eXchange Top of stack with H and L)
SPHL		(move H and L to SP)
OUT	PORT	(OUTput from port address)
IN	PORT	(INput from port address)
DI		(Disable Interrupts)
EI		(Enable Interrupts)
NOP		(No OPeration)
HLT		(HaLT)